What I claim is:

1. A micro-controller controlling a data transfer to or from a host device through a pair of data lines for transferring a first data at the first data line and a second data at the second data line, which is different from the first data respectively, comprising:

an internal circuit;

a transfer control unit, which is operated in response to a oscillation signal, watching a condition of the data transfer at the pair of the data lines, and outputting a first output signal as a watching result, the transfer control unit having a function for receiving the first data and the second data and transferring a desired data to the host device through the pair of data lines;

a main control unit, which is operated by the oscillation signal, receiving the first output signal from the transfer control unit, and controlling an operation of the internal circuit in response to the first output signal, the main control unit changing its mode from an operative mode to an inoperable mode or from the inoperative mode to the operable mode in response to the watching result, and the main control unit outputting a second signal when the main control unit is in the inoperative mode; and

an oscillating circuit generating the oscillation signal having a frequency, the oscillating circuit being inactivated in response to the second signal, and the oscillating circuit being activated in response to the watching result when the main control unit returns to the operable mode.

2. A micro-controller, as claimed in claim 1, wherein the frequency of the oscillation signal is a first frequency, further comprising a clock signal generating circuit, which generates a clock signal having a second frequency that is higher than the first frequency by receiving the oscillation signal and sends the clock signal to the transfer control unit, the transfer control unit being operated by the clock signal.

3. A micro-controller, as claimed in claim 2 wherein the operation of the clock signal generating circuit is controlled in response to the watching result.

4. A micro-controller, as claimed in claim 1 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to be in the inoperable mode when transfer control unit detects the condition showing that the voltage level of the first data is at the first level and the voltage level of the second data is at the second level, which is different from the first level, for a particular period.

5. A micro-controller, as claimed in claim 4 wherein the transfer control unit sends the oscillating circuit the watching result for instructing the generation of the oscillation signal by detecting the condition showing that the voltage level of the first data is at the second level and the voltage level of the second data is at the

first level while the main control unit is in the inoperable mode.

6. A micro-controller, as claimed in claim 5 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to return to the operable mode when the transfer control unit detects the condition for a particular period showing that the voltage levels of the first and second data are at the second level.

7. A micro-controller, as claimed in claim 5, further including a switch circuit selecting a first choice that a power supply voltage of the main control circuit is supplied from the host device when the host is connected to the pair of the data lines, or selecting a second choice that a power supply voltage of the main control circuit is supplied from an external power supply voltage generating circuit when the host is connected to the pair of the data lines, the selection being made by a detection of the condition whether the host device is connected to the pair of the data lines, and the detection being made by a voltage level of a voltage supplied from the host device.

8. A micro-controller, as claimed in claim 7, further including an OR gate controlling to apply the watching result for instructing the generation of the oscillation signal to the oscillating circuit.

9. A micro-controller, as claimed in claim 2 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to be in the inoperable mode when the transfer control unit detects the condition showing that the voltage level of the first data is at the first level and the voltage level of the second data is at the second level, which is different from the first level, for a particular period.

10. A micro-controller, as claimed in claim 9 wherein the transfer control unit sends the oscillating circuit the watching result for instructing the generation of the oscillation signal by detecting the condition showing that the voltage level of the first data is at the second level and the voltage level of the second data is at the first level while the main control unit is in the inoperable mode.

11. A micro-controller, as claimed in claim 10 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to return to the operable mode when transfer control unit detects the condition for a particular period showing that the voltage levels of the first and second data are at the second level.

12. A micro-controller, as claimed in claim 3 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to be in the inoperable mode when transfer control unit detects the

condition showing that the voltage level of the first data is at the first level and the voltage level of the second data is at the second level, which is different from the first level, for a particular period.

13. A micro-controller, as claimed in claim 12 wherein the transfer control unit sends the oscillating circuit the watching result for instructing the generation of the oscillation signal by detecting the condition showing that the voltage level of the first data is at the second level and the voltage level of the second data is at the first level while the main control unit is in the inoperable mode.

14. A micro-controller, as claimed in claim 13 wherein the transfer control unit sends the main control unit the watching result showing that the main control unit is allowed to return to the operable mode when transfer control unit detects the condition for a particular period showing that the voltage levels of the first and second data are at the second level.

15. A micro-controller, as claimed in claim 1 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

16. A micro-controller, as claimed in claim 2 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

17. A micro-controller, as claimed in claim 3 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

18. A micro-controller, as claimed in claim 4 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

19. A micro-controller, as claimed in claim 5 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

20. A micro-controller, as claimed in claim 6 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

21. A micro-controller, as claimed in claim 7 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

22. A micro-controller, as claimed in claim 8 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.

23. A micro-controller, as claimed in claim 10 wherein the transfer control unit and the main control unit are formed on a single semiconductor chip.